

***Amendments to the Claims***

The listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (currently amended): A cache controller for use with a processor, comprising:

a plurality of mappers for receiving instructions of ~~a first~~ an instruction set, each mapper for mapping an instruction of said ~~first~~ instruction set to a predetermined instruction width format (PIWF) configuration; and

a multiplexor for receiving said PIWF configurations from said plurality of mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor.

Claim 2 (original): The cache controller of claim 1, further comprising:

a tag comparator for generating said selector signal.

Claim 3 (currently amended): The cache controller of claim 2, wherein said tag comparator comprises:

means for comparing, for each instruction provided to one of said plurality of mappers, a tag associated with an instruction of said ~~first~~ instruction set to a desired tag and generating said selector signal to cause said multiplexor to select said desired one of said PIWF configurations.

Claim 4 (original): The cache controller of claim 3, wherein said plurality of mappers comprise:

at least one first mapper for receiving instructions from a fill buffer; and

at least one second mapper for receiving instructions from an instruction cache.

Claim 5 (currently amended): In a cache controller for use with a processor, a method for mapping ~~a first an~~ instruction set to a predetermined instruction width format (PIWF) configuration, comprising:

- (a) reading instructions of said ~~first~~ instruction set from an instruction cache into a plurality of mappers, each instruction of said ~~first~~ instruction set being read into a corresponding one of said plurality of mappers in preparation for mapping;
- (b) mapping each instruction of said ~~first~~ instruction set to a corresponding PIWF configuration; and
- (c) selecting a desired one of said PIWF configurations for decoding and execution by the processor.

Claim 6 (currently amended): The method of claim 5, further comprising the step of:

- (d) comparing, for each instruction provided to said plurality of mappers, a tag associated with an instruction of said ~~first~~ instruction set to a desired tag, wherein said desired one of said mapped instructions is selected based on said comparison.

Claim 7 (currently amended): The method of claim 5, wherein step (a) further comprises:

(d) reading an instruction from a fill buffer into a corresponding one of said plurality of mappers.

Claim 8 (currently amended): A processor comprising:

an execution unit;

a decoder;

a cache for storing ~~said~~ instructions; and

a cache controller for retrieving ~~said~~ instructions from ~~said~~ cache and providing ~~said~~ instructions to ~~said instruction~~ decoder, ~~said~~ cache controller comprising:

a plurality of mappers for mapping a plurality of instructions of ~~a first an~~ instruction set to predetermined instruction width format (PIWF) configurations,

a multiplexor for selecting, in response to a selector signal, one of said PIWF configurations for decoding by ~~said~~ decoder and execution by ~~said~~ execution unit, and

means for comparing, for each instruction provided to ~~said~~ multiplexor, a tag associated with an instruction of ~~said first~~ instruction set to a desired tag and generating ~~said~~ selector signal to cause ~~said~~ multiplexor to select ~~said desired one of said~~ PIWF configurations,

whereby ~~said~~ processor performs instruction mapping substantially in parallel with tag comparison to improve processor performance.

Claim 9 (original): The processor of claim 8, wherein said plurality of mappers comprise:

at least one first mapper for receiving instructions from a fill buffer; and at least one second mapper for receiving instructions from said instruction cache.

Claim 10 (currently amended): A computer readable medium comprising a microprocessor core embodied in software, the microprocessor core including a cache controller comprising:

a plurality of mappers for receiving instructions of ~~a first~~ an instruction set, each mapper for mapping an instruction of said ~~first~~ instruction set to a predetermined instruction width format (PIWF) configuration; and

a multiplexor for receiving said PIWF configurations from said plurality of mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor.